AMENDMENTS TO THE CLAIMS:

This listing of claims will replace all prior versions, and listings, of claims in the application:

Listing of Claims:

Claims 1-5 (canceled).

6. (New) A control unit having an oscillator for a processor (μC), the control unit being configured so that the control unit stores a temporary absence of oscillation of the oscillator in a first error memory (15), if oscillation begins again after the absence.

7. (New) The control unit according to Claim 6, wherein the control unit has a logic module (PIC, 10, 12, 13) which, when oscillation is absent, sets a second error memory (14) to a predefined state, the logic module storing the absence in the first error memory (15) as a function of the state of the second error memory (14) and the resuming of oscillation.

8. (New) The control unit according to Claim 7, wherein a timer module (10) is assigned to the logic module in such a way that after a predefined time after the supply voltage is turned on, the second error memory (14) is set to the state if the oscillation is then still absent.

9. (New) The control unit according to Claim 7, wherein the control unit is configured in such a way that the control unit resets the second memory (14) after oscillation has begun again.

10. (New) The control unit according to Claim 8, wherein the control unit is configured in such a way that the

control unit resets the second memory (14) after oscillation has begun again.

11. (New) The control unit according to Claim 7, wherein the logic module continues to generate a signal that identifies the absence of oscillation until the second error memory is reset.

12. (New) The control unit according to Claim 8, wherein the logic module continues to generate a signal that identifies the absence of oscillation until the second error memory is reset.

13. (New) The control unit according to Claim 9, wherein the logic module continues to generate a signal that identifies the absence of oscillation until the second error memory is reset.

14. (New) The control unit according to Claim 10, wherein the logic module continues to generate a signal that identifies the absence of oscillation until the second error memory is reset.